96, 99, 372.2; 428/428, 457, 688, 689, 901 [IMAGE AVAILABLE]

3. 4,954,214, Sep. 4, 199[redacted] Method for making interconnect structures for VLSI devices; Vu Quoc Ho, 156/628, 652, 653, 655, 656, 657; 437/228 [IMAGE AVAILABLE]

4. 4,619,887, Oct. 28, 1986, Method of Plating an interconnect metal onto a metal in VLSI devices; Robert C. Hooper, et al., 430/313; 156/642; 205/125; 430/314, 315, 316, 317, 318, 319

5. 4,614,119, Sep. 30, 1986, Resonant hollow beam and method; Paul M. Zavracky, et al., 73/704, 715, 754; 156/628, 630, 633, 634, 647, 651, 656, 657, 662



6. 4,613,314, Sep. 23, 1986, Ionization detector; Douglas S. Steele, 445/28; 156/645; 445/35, 59

7. 4,613,313, Sep. 23, 1986, Ionization detector; Douglas S. Steele, 445/28; 29/446; 156/634; 250/374, 385.1; 445/35, 59

8. 4,528,064, Jul. 9, 1985, Method of making multilayer circuit board; Kenji Ohsawa, et al., 156/630; 29/852; 156/634, 644, 902; 174/261; 427/97 [IMAGE AVAILABLE]

9. 4,404,059, Sep. 13, 1983, Process for manufacturing panels to be used in microelectronic systems; Vladimir I. Livshits, et al., 156/629; 29/846; 156/151, 630, 634, 651, 656, 902; 174/253; 205/125 [IMAGE AVAILABLE]



10. 4,321,284, Mar. 23, 1982, Manufacturing method for semiconductor device; Hisao Yakushiji, 437/194; 156/643, 653, 657; 427/96; 430/314; 437/203

11. 4,022,931, May 10, 1977, Process for making semiconductor device; James R. Black, et al., 437/187; 156/654, 655; 357/65, 67, 68; 437/182, 188, 199

12. 3,994,793, Nov. 30, 1976, Reactive ion etching of aluminum; Joseph M. Harvilchuck, et al., 204/192.25; 156/646; 204/164, 192.15, 192.22; 219/121.4, 121.41 [IMAGE AVAILABLE]

13. 3,957,552, May 18, 1976, Method for making multilayer devices using only a single critical masking step; Kie Y. Ahn, et al., 156/651, 656, 661.1; 427/131, 259, 264, 265, 552, 553; 430/312; 437/187, 228



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12. 4,842,891, Jun. 27, 1989, Method of forming a copper film by chemical vapor deposition; Hiroshi Miyazaki, et al., 427/569, 252, 584, 585; 437/245

13. 4,810,620, Mar. 7, 1989, Nickel plated tape; Hem P. Takiar, et al., 430/314; 205/135; 357/69, 70; 430/318, 320; 437/220



14. 4,746,621, May 24, 1988, Planar tungsten interconnect; David C. Thomas, et al., 437/24, 37, 195, 200

15. 4,742,014, May 3, 1988, Method of making metal contacts and interconnections for VLSI devices with copper as a primary conductor; Robert C. Hooper, et al., 437/192, 198, 200, 203

16. 4,707,418, Nov. 17, 1987, Nickel plated copper tape; Hem P. Takiar, et al., 428/675; 228/180.2; 357/70; 437/220

17. 4,648,175, Mar. 10, 1987, Use of selectively deposited tungsten for contact formation and shunting metallization; Werner A. Metz, Jr., et al., 437/192; 357/2, 23.1, 23.9, 42, 59, 71; 437/193, 245

18. 4,630,357, Dec. 23, 1986, Method for forming improved contacts between interconnect layers of an integrated circuit; Steven H. Rogers, et al., 437/189, 192, 195, 200



19. 4,321,284, Mar. 23, 1982, Manufacturing method for semiconductor device; Hisao Yakushiji, 437/194; 156/643, 653, 657; 427/96; 430/314; 437/203

20. 4,310,568, Jan. 12, 1982, Method of fabricating improved Schottky barrier contacts; James K. Howard, et al., 437/175; 204/192.15

21. 4,260,428, Apr. 7, 1981, Photovoltaic cell; Pradip K. Roy, 136/260; 205/162, 164, 178, 183; 357/30; 427/74; 437/5

22. 4,022,931, May 10, 1977, Process for making semiconductor device; James R. Black, et al., 437/187; 156/654, 655; 357/65, 67, 68; 437/182, 188, 199

23. 3,957,552, May 18, 1976, Method for making multilayer devices using only a single critical masking step; Kie Y. Ahn, et al., 156/651, 656, 661.1;



427/131, 259, 264, 265, 552, 553; 430/312; 437/187, 228

24. 3,932,685, Jan. 13, 1976, Aluminum stabilization process and stabilization solution therefor; Dervin L. Flowers, 427/352; 106/1.23, 1.24; 427/380, 383.7, 436; 437/194, 230

25. 3,747,202, Jul. 24, 1973, METHOD OF MAKING BEAM LEADS ON SUBSTRATES; John Robert Jordan, 437/182; 357/69; 437/192, 226, 246

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L25 13 L21 AND L23

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1. 5,152,864, Oct. 6, 1992, Method of manufacturing surface acoustic wave device; Hideharu Ieki, et al., 156/610; 310/313B, 313R; 427/100, 126.4 [IMAGE AVAILABLE]



2. 4,963,423, Oct. 16, 19[redacted], Method for forming a th[redacted] film and apparatus of forming a metal thin film utilizing temperature controlling means; Atsushi Sakiyuchi, et al., 428/209; [redacted], 174/250; 361/397; 427/58

L13 1116 S L10 AND L12
L14 570567 S METAL
L15 973 S L13 AND [redacted]4
L16 403190 S VIA#
17 DEC 92 10:47:59 U.S. Patent & Trademark Office P0050
L17 24205 S MULTILAYER OR MULTI-LAYER
L18 307 S L15 AND L17
L19 15824 S 437/CLAS
L20 70 S L18 AND L19
L21 70874 S 156/CLAS
L22 50 S L18 AND L21

=> s l1 and l3
L23 90 L1 AND L3

=> s l19 and l23
L24 25 L19 AND L23

=> d 1-25

1. 5,171,713, Dec. 15, 1992, Process for forming planarized, air-bridge interconnects on a semiconductor substrate; James A. Matthews, 437/189; 17 DEC 92 10:50:26 U.S. Patent & Trademark Office P0051 148/DIG.20; 257/750; 437/183, 195, 228 [IMAGE AVAILABLE]

2. 5,134,083, Jul. 28, 1992, Method of forming self-aligned contacts in a semiconductor process; James A. Matthews, 437/40; 148/DIG.19; 437/31, 56, 193, 200, 228 [IMAGE AVAILABLE]

3. 5,132,237, Jul. 21, 1992, Planarization method for fabricating high density semiconductor devices; James A. Matthews, 437/40, 41, 50, 67, 193, 228 [IMAGE AVAILABLE]

4. 5,112,761, May 12, 1992, BiCMOS process utilizing planarization technique; James A. Matthews, 437/31; 357/43; 437/34, 44, 50, 57, 162, 193, 200, 228 [IMAGE AVAILABLE]

5. 5,108,945, Apr. 28, 1992, Process for fabricating polysilicon resistors and interconnects; James A. Matthews, 437/60; 148/DIG.136; 437/41, 59, 193, 918 [IMAGE AVAILABLE]
17 DEC 92 10:50:38 U.S. Patent & Trademark Office P0052

6. 5,087,590, Feb. 11, 1992, Method of manufacturing semiconductor devices; Hitoshi Fujimoto, et al., 437/209; 148/DIG.17; 361/421; 428/620; 437/210, 220 [IMAGE AVAILABLE]

7. 5,075,756, Dec. 24, 1991, Low resistance contacts to semiconductor materials; Ranjan Dutta, 357/67, 65; 437/180, 184 [IMAGE AVAILABLE]

8. 5,011,792, Apr. 30, 1991, Method of making ohmic resistance WSb, contacts to III-V semiconductor materials; Ranjan Dutta, 437/184; 148/DIG.20; 357/65, 67; 437/192 [IMAGE AVAILABLE]

9. 4,962,060, Oct. 9, 1990, Making a high speed interconnect system with refractory non-dogbone contacts and an active electromigration suppression mechanism; Jack Sliwa, et al., 437/192; 357/67; 428/651 [IMAGE AVAILABLE]
17 DEC 92 10:50:48 U.S. Patent & Trademark Office P0053

10. 4,954,214, Sep. 4, 1990, Method for making interconnect structures for VLSI devices; Vu Quoc Ho, 156/628, 652, 653, 655, 656, 657; 437/228 [IMAGE AVAILABLE]

11. 4,943,539, Jul. 24, 1990, Process for making a multilayer metallization structure; Syd R. Wilson, et al., 437/195, 192, 228, 947
[IMAGE AVAILABLE]

205/187, 222; 427/259, 282, 306, 307, 322, 443.1; 437/230



59. 4,143,385, Mar. 6, 1979, Photocoupler; Tadahiko Miyoshi, et al., 357/19; 250/551; 357/17, 65, 67, 68, 75; 437/5

60. 4,095,330, Jun. 20, 1978, Composite semiconductor integrated circuit and method of manufacture; Chung K. Kim, 437/86, 167, 205, 245, 249, 904

61. 4,075,756, Feb. 28, 1978, Process for fabricating above and below ground plane wiring on one side of a supporting substrate and the resulting circuit configuration; Charles John Kircher, et al., 29/847; 307/245; 427/63; 437/51, 180, 190; 505/923

62. 4,052,787, Oct. 11, 1977, Method of fabricating a beam lead flexible circuit; Joseph M. Shaheen, et al., 29/827, 847; 156/631, 634; 205/125; 427/98; 430/314, 414; 437/182, 203, 245



63. 4,022,931, May 10, 1977, Process for making semiconductor device; James R. Black, et al., 437/187; 156/654, 655; 357/65, 67, 68; 437/182, 188, 199

64. 3,952,404, Apr. 27, 1976, Beam lead formation method; Mituo Matunami, 437/182; 357/69; 437/9, 246

65. 3,930,857, Jan. 6, 1976, Resist process; Diana Jean Bendz, et al., 430/313; 156/651; 427/96, 259; 430/312, 314, 315, 316, 318, 323, 324, 329; 437/229

66. 3,905,094, Sep. 16, 1975, Thermal display module; Edward M. Ruggiero, 437/205; 357/45, 49; 437/60, 211, 226, 249

67. 3,771,219, Nov. 13, 1973, METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE; Takateru Tuzi, et al., 437/182; 357/54, 69



68. 3,751,292, Aug. 7, 1973, MULTILAYER METALLIZATION SYSTEM; Lowell S. Kongable, 357/69; 29/825; 156/656; 205/186; 357/71; 437/182, 192

69. 3,698,082, Oct. 17, 1972, COMPLEX CIRCUIT ARRAY METHOD; Tom M. Hyltin, et al., 29/856; 264/272.17; 357/74; 437/209

70. 3,617,824, Nov. 2, 1971, MOS DEVICE WITH A METAL-SILICIDE GATE; Daizaburo Shinoda, et al., 357/23.1; 148/DIG.53, DIG.139, DIG.147; 357/41, 48, 52, 67; 437/142

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L1 27692 S PLATING
L2 156293 S STRESS##
L3 825 S ELECTRO(W)MIGRATION OR ELECTROMIGRATION
L4 5161 S L1 AND L2
L5 90 S L1 AND L3
L6 39 S L4 AND L5
L7 218349 S ALUMINUM
L8 9792 S L1 AND L7
L9 244010 S INTERCONNECT###
L10 4566 S L1 AND L
L11 82 S SEMCONDUCTOR
L12 8744 S SEMICONDUCTOR

43. 4,6Ø9,567, Sep. 2, 1986, High efficiency stable CdS-Cu.sub.2 S solar cells manufacturing proces[redacted]using thick film methodol[redacted]; Ottilia F. Toth, et al., 427/74; 136/258, 26Ø, [redacted]65; 437/4, 965

44. 4,6Ø4,791, Aug. 12, 1986, Method for producing multi-layer, thin-film, flexible silicon alloy photovoltaic cells; William J. Todorof, 437/4; 148/557; 156/6Ø8, DIG.88; 264/332; 437/248

45. 4,562,Ø92, Dec. 31, 1985, Method of fabricating complex microcircuit boards, substrates and microcircuits and the substrates and microcircuits; Raymond E. Wiech, Jr., 427/58; 264/61; 427/96, 1Ø1, 287, 374.4; 437/188, 247, 918

46. 4,479,Ø27, Oct. 23, 1984, Multi-layer thin-film, flexible silicon alloy photovoltaic cell; William J. Todorof, 136/249, 255, 256, 257,



258, 259, 261; 252/62.3BT, 62.3R, 5Ø1.1; 357/3Ø; 437/2

47. 4,445,267, May 1, 1984, MOSFET Structure and process to form micrometer long source/drain spacing; Francisco H. De La Moneda, et al., 437/41; 357/23.3; 437/42, 44, 56, 7Ø, 195, 2ØØ

48. 4,419,8Ø9, Dec. 13, 1983, Fabrication process of sub-micrometer channel length MOSFETs; Jacob Riseman, et al., 437/41; 156/654; 357/23.3, 23.9; 437/27, 44, 7Ø, 193, 2ØØ, 2Ø1, 931

49. 4,4ØØ,865, Aug. 3Ø, 1983, Self-aligned metal process for integrated circuit metallization; George R. Goth, et al., 437/31; 156/643, 656; 357/34, 36, 59; 437/33, 39, 69, 194, 195, 2Ø3, 931

5Ø. 4,396,457, Aug. 2, 1983, Method of making bumped-beam tape; Frank C.



Bakermans, 437/183; 156/634, 645, 656, 9Ø2; 357/7Ø; 437/22Ø, 221

51. 4,372,996, Feb. 8, 1983, Method for metallizing aluminum pads of an integrated circuit chip; Elis A. Guditz, et al., 437/23Ø; 1Ø6/1.29; 427/436; 437/194, 229

52. 4,35Ø,99Ø, Sep. 21, 1982, Electrode for lead-salt diodes; Wayne Lo, 357/16, 17, 3Ø, 52, 61, 62, 63, 67, 71; 437/165, 189, 246, 9Ø6, 946, 987

53. 4,347,655, Sep. 7, 1982, Mounting arrangement for semiconductor optoelectronic devices; Peter S. Zory, et al., 437/218; 357/8Ø, 81; 437/9Ø8

54. 4,344,223, Aug. 17, 1982, Monolithic hybrid integrated circuits; Gary A. Bulger, et al., 437/54; 2Ø5/124; 437/192, 247



55. 4,339,3Ø5, Jul. 13, 1982, Planar circuit fabrication by plating and liftoff; Addison B. Jones, 156/65Ø, 655, 657, 659.1, 668; 2Ø4/192.3, 192.32; 357/71; 365/37, 39; 427/131; 43Ø/313, 317; 437/189, 2Ø3, 23Ø, 245

56. 4,321,284, Mar. 23, 1982, Manufacturing method for semiconductor device; Hisao Yakushiji, 437/194; 156/643, 653, 657; 427/96; 43Ø/314; 437/2Ø3

57. 4,179,8Ø2, Dec. 25, 1979, Studded chip attachment process; Kailash C. Joshi, et al., 437/183; 29/83Ø, 843, 847; 228/18Ø.2, 254; 437/2Ø9; 5Ø5/923, 927

58. 4,15Ø,177, Apr. 17, 1979, Method for selectively nickeling a layer of polymerized polyester resin; Elis A. Guditz, et al., 43Ø/324; 156/645, 668;

148/DIG.20, DIG.164; 156/643, 644, 646; 437/195, 203, 915, 978

29. 4,835,120, May 30, 1989, Method of making a multilayer molded plastic IC package; Debendra Mallik, et al., 437/209; 174/52.2; 264/272.11; 437/220, 224 [IMAGE AVAILABLE]

30. 4,771,013, Sep. 13, 1988, Process of making a double heterojunction 3-D I.sup.2 L bipolar transistor with a Si/Ge superlattice; Patrick A. Curran, 437/31; 148/DIG.11, DIG.12, DIG.142, DIG.147, DIG.160, DIG.164, DIG.169; 156/613, 614; 357/34, 56, 92; 437/55, 106, 110, 111, 131,
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174, 200

31. 4,770,897, Sep. 13, 1988, Multilayer interconnection system for multichip high performance semiconductor packaging; Andrew L. Wu, 437/228; 204/192.1; 427/98, 510, 520; 430/310, 313, 314, 315, 329

32. 4,766,670, Aug. 30, 1988, Full panel electronic packaging structure and method of making same; Charles E. Gazdik, et al., 29/830, 593, 840; 361/398; 437/205 [IMAGE AVAILABLE]

33. 4,753,851, Jun. 28, 1988, Multiple layer, tungsten/titanium/titanium nitride adhesion/diffusion barrier layer structure for gold-base microcircuit interconnection; Bruce E. Roberts, et al., 428/627; 204/192.17; 357/71; 427/123; 428/620, 628, 641, 660, 665, 672; 437/246

34. 4,746,621, May 24, 1988, Planar tungsten interconnect; David C. Thomas, et al., 437/24, 37, 195, 200
17 DEC 92 10:46:03 U.S. Patent & Trademark Office P0040

35. 4,732,865, Mar. 22, 1988, Self-aligned internal mobile ion getter for multi-layer metallization on integrated circuits; David R. Evans, et al., 437/12, 192

36. 4,722,914, Feb. 2, 1988, Method of making a high density IC module assembly; James E. Drye, et al., 437/213; 29/740; 156/644, 662; 174/52.2; 357/73; 437/981, 982 [IMAGE AVAILABLE]

37. 4,717,681, Jan. 5, 1988, Method of making a heterojunction bipolar transistor with SIPOS; Patrick A. Curran, 437/31; 156/614; 357/16, 34, 55, 59, 60, 67; 437/68, 106, 126, 196, 203

38. 4,708,904, Nov. 24, 1987, Semiconductor device and a method of manufacturing the same; Masahiro Shimizu, et al., 428/209; 156/656, 657; 204/192.34; 427/96; 428/901; 430/396; 437/192, 200, 946
17 DEC 92 10:46:14 U.S. Patent & Trademark Office P0041

39. 4,702,967, Oct. 27, 1987, Multiple-layer, multiple-phase titanium/nitrogen adhesion/diffusion barrier layer structure for gold-base microcircuit interconnection; Jimmy C. Black, et al., 428/620; 204/192.17; 357/71; 428/627, 660, 673; 437/246

40. 4,654,113, Mar. 31, 1987, Process for fabricating a semiconductor device; Takahiro Tuchiya, et al., 156/643, 644, 646, 653, 657, 659.1, 661.1, 668, 904; 437/186, 187, 191

41. 4,631,805, Dec. 30, 1986, Semiconductor device including plateless package fabrication method; Dennis R. Olsen, et al., 437/211, 9, 217

42. 4,630,357, Dec. 23, 1986, Method for forming improved contacts between interconnect layers of an integrated circuit; Steven H. Rogers, et al.,
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437/189, 192, 195, 200

al., 357/71; 437/203 [IMAGE AVAILABLE]

14. 5,096,852, Mar. 17, 1992, Method of making plastic encapsulated multichip hybrid integrated circuits; Larry D. Hobson, 437/207, 220 [IMAGE AVAILABLE]

15. 5,093,282, Mar. 3, 1992, Method of making a semiconductor device

having lead pins and a metal shell; Jun-ichi Ohno, et al., 437/221; 174/52.4; 437/245, 915 [IMAGE AVAILABLE]

16. 5,066,614, Nov. 19, 1991, Method of manufacturing a leadframe having conductive elements preformed with solder bumps; Thomas J. Dunaway, et al., 437/209; 357/67, 74; 437/215, 216, 217, 220 [IMAGE AVAILABLE]

17. 5,055,427, Oct. 8, 1991, Process of forming self-aligned interconnects for semiconductor devices; Jacob D. Haskell, 437/203, 46, 186, 187, 228 [IMAGE AVAILABLE]

18. 5,036,016, Jul. 30, 1991, VLSI bipolar transistor process; Robert M. Drosd, 437/31; 148/DIG.10, DIG.11, DIG.96; 437/26, 32, 909, 917 [IMAGE AVAILABLE]

19. 5,028,555, Jul. 2, 1991, Self-aligned semiconductor devices; Jacob

D. Haskell, 437/57; 148/DIG.50, DIG.141; 357/23.5, 23.9; 437/40, 41, 228, 233, 984 [IMAGE AVAILABLE]

20. 4,997,778, Mar. 5, 1991, Process for forming a self-aligned FET having a T-shaped gate structure; Kyunhwan Sim, et al., 437/40; 148/DIG.100; 437/41, 44, 187, 203, 912 [IMAGE AVAILABLE]

21. 4,997,517, Mar. 5, 1991, Multi-metal layer interconnect tape for tape automated bonding; Arvind Parthasarathi, 156/630; 29/827; 156/634, 644, 656, 659.1, 901; 437/220 [IMAGE AVAILABLE]

22. 4,977,108, Dec. 11, 1990, Method of making self-aligned, planarized contacts for semiconductor devices; Jacob D. Haskell, 437/229; 148/DIG.50, DIG.141; 437/41, 56, 193, 228 [IMAGE AVAILABLE]

23. 4,943,539, Jul. 24, 1990, Process for making a multilayer

metallization structure; Syd R. Wilson, et al., 437/195, 192, 228, 947 [IMAGE AVAILABLE]

24. 4,872,947, Oct. 10, 1989, CVD of silicon oxide using TEOS decomposition and in-situ planarization process; David N. Wang, et al., 156/643; 118/50.1, 620, 728; 156/345, 646, 653, 657; 204/192.12, 192.37, 298.33, 298.35; 427/248.1, 294, 574, 585; 437/235, 238

25. 4,866,001, Sep. 12, 1989, Very large scale bipolar integrated circuit process; James M. Pickett, et al., 437/32; 148/DIG.10, DIG.11; 357/35, 59; 437/33, 228, 241

26. 4,859,633, Aug. 22, 1989, Process for fabricating monolithic microwave diodes; Burhan Bayraktaroglu, 437/211; 357/51, 81; 437/107, 184, 192, 902, 904


27. 4,857,482, Aug. 15, 1989, Method of forming bump electrode and electronic circuit device; Masayuki Saito, et al., 437/209; 29/739, 837; 206/329; 264/272.11; 357/74

28. 4,840,923, Jun. 20, 1989, Simultaneous multiple level interconnection process; Denis G. Flagello, et al., 437/189;

49. 3,779,841, Dec. 18, 1973, FABRICATION OF THIN FILM RESISTOR CROSSOVERS

FOR INTEGRATED CIRCUITS; Thomas J. Sanders, 156/650; 357/51, 68

50. 3,751,292, Aug. 7, 1973, MULTILAYER METALLIZATION SYSTEM; Lowell S. Kongable, 357/69; 29/825; 156/656; 205/186; 357/71; 437/182, 192

=> d 1-70 120

1. 5,171,713, Dec. 15, 1992, Process for forming planarized, air-bridge interconnects on a semiconductor substrate; James A. Matthews, 437/189; 148/DIG.20; 257/750; 437/183, 195, 228 [IMAGE AVAILABLE]

2. 5,171,711, Dec. 15, 1992, Method of manufacturing integrated circuit devices; Hiroshi Tobimatsu, 437/182; 148/DIG.100; 437/192, 209, 944 [IMAGE AVAILABLE]

3. 5,162,258, Nov. 10, 1992, Three metal personalization of application

specific monolithic microwave integrated circuit; Zachary J. Lemnios, et al., 437/184; 257/296, 528; 437/47, 51, 60, 195, 919 [IMAGE AVAILABLE]

4. 5,156,983, Oct. 20, 1992, Method of manufacturing tape automated bonding semiconductor package; Randall L. Schlesinger, et al., 437/8; 29/830; 324/158F; 437/206, 217, 220 [IMAGE AVAILABLE]

5. 5,138,430, Aug. 11, 1992, High performance versatile thermally enhanced IC chip mounting; John Gow, 3rd, et al., 357/70, 71, 72, 81; 437/207, 209, 217, 219 [IMAGE AVAILABLE]

6. 5,134,083, Jul. 28, 1992, Method of forming self-aligned contacts in a semiconductor process; James A. Matthews, 437/40; 148/DIG.19; 437/31, 56, 193, 200, 228 [IMAGE AVAILABLE]

7. 5,132,237, Jul. 21, 1992, Planarization method for fabricating high

density semiconductor devices; James A. Matthews, 437/40, 41, 50, 67, 193, 228 [IMAGE AVAILABLE]

8. 5,118,361, Jun. 2, 1992, Terrestrial concentrator solar cell module; Lewis M. Fraas, et al., 136/246, 244, 249, 251; 437/2, 5 [IMAGE AVAILABLE]

9. 5,112,761, May 12, 1992, BiCMOS process utilizing planarization technique; James A. Matthews, 437/31; 357/43; 437/34, 44, 50, 57, 162, 193, 200, 228 [IMAGE AVAILABLE]

10. 5,112,448, May 12, 1992, Self-aligned process for fabrication of interconnect structures in semiconductor applications; Kishore K. Chakravorty, 205/118; 156/643, 652, 659.1; 205/182, 223, 224, 917; 437/192, 228 [IMAGE AVAILABLE]


11. 5,108,945, Apr. 28, 1992, Process for fabricating polysilicon resistors and interconnects; James A. Matthews, 437/60; 148/DIG.136; 437/41, 59, 193, 918 [IMAGE AVAILABLE]

12. 5,103,557, Apr. 14, 1992, Making and testing an integrated circuit using high density probe points; Glenn J. Leedy, 29/832, 407, 846; 324/158F; 437/8 [IMAGE AVAILABLE]

13. 5,103,288, Apr. 7, 1992, Semiconductor device having multilayered wiring structure with a small parasitic capacitance; Mitsuru Sakamoto, et

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34. 4,359,Ø12, Nov. 16, 1982, Apparatus for producing a semiconductor device utlizing successive liquid growth; Jun-ichi Nishizawa, 118/59, 412, 415; 156/622

35. 4,339,3Ø5, Jul. 13, 1982, Planar circuit fabrication by plating and liftoff; Addison B. Jones, 156/650, 655, 657, 659.1, 668; 2Ø4/192.3, 192.32; 357/71; 365/37, 39; 427/131; 43Ø/313, 317; 437/189, 2Ø3, 23Ø, 245

36. 4,336,Ø88, Jun. 22, 1982, Method of fabricating an improved multi-layer ceramic substrate; Richard J. Hetherington, et al., 156/89; 29/851; 174/253, 264; 361/4Ø6, 411 [IMAGE AVAILABLE]



37. 4,321,284, Mar. 23, 1982, Manufacturing method for semiconductor device; Hisao Yakushiji, 437/194; 156/643, 653, 657; 427/96; 43Ø/314; 437/2Ø3

38. 4,315,985, Feb. 16, 1982, Fine-line circuit fabrication and photoresist application therefor; Eugene E. Castellani, et al., 43Ø/314; 156/659.1; 2Ø5/125, 135; 427/16Ø, 346; 43Ø/318, 323, 324, 327, 33Ø, 935

39. 4,279,69Ø, Jul. 21, 1981, High-radiance emitters with integral microlens; Eugene G. Dierschke, 156/649, 648, 654, 656, 662; 313/11Ø, 498, 499; 357/17; 427/77

4Ø. 4,253,9Ø7, Mar. 3, 1981, Anisotropic plasma etching; Peter D. Parry, et al., 156/643, 646, 656, 657, 659.1; 2Ø4/192.32, 298.33, 298.34; 219/121.41, 121.42, 121.43; 422/186.Ø5, 186.29 [IMAGE AVAILABLE]

41. 4,249,3Ø2, Feb. 1Ø, 1981, Multilayer printed circuit board; Philip



C. Crepeau, 29/83Ø, 852; 156/625, 9Ø1; 361/414; 427/97; 428/138, 9Ø1; 439/74, 77 [IMAGE AVAILABLE]

42. 4,159,222, Jun. 26, 1979, Method of manufacturing high density fine line printed circuitry; Sanford Lebow, et al., 156/632, 153, 233, 249, 289, 631, 645, 9Ø2; 2Ø5/78; 427/96, 264, 282, 4Ø9

43. 4,15Ø,177, Apr. 17, 1979, Method for selectively nickeling a layer of polymerized polyester resin; Elis A. Guditz, et al., 43Ø/324; 156/645, 668; 2Ø5/187, 222; 427/259, 282, 3Ø6, 3Ø7, 322, 443.1; 437/23Ø

44. 4,Ø52,787, Oct. 11, 1977, Method of fabricating a beam lead flexible circuit; Joseph M. Shaheen, et al., 29/827, 847; 156/631, 634; 2Ø5/125; 427/98; 43Ø/314, 414; 437/182, 2Ø3, 245

45. 4,Ø22,931, May 1Ø, 1977, Process for making semiconductor device;



James R. Black, et al., 437/187; 156/654; 655; 357/65, 67, 68; 437/182, 188, 199

46. 4,Ø12,3Ø7, Mar. 15, 1977, Method for conditioning drilled holes in multilayer wiring boards; Eugene Phillips, 2Ø4/192.32; 29/851, 852; 156/643, 644; 174/259, 264; 2Ø4/164 [IMAGE AVAILABLE]

47. 3,965,277, Jun. 22, 1976, Photoformed plated interconnection of embedded integrated circuit chips; Elis A. Guditz, et al., 43Ø/319; 156/3ØØ, 645, 65Ø, 655, 668; 264/272.17; 427/98, 272, 4Ø5, 4Ø9, 51Ø; 43Ø/269, 315, 396

48. 3,93Ø,857, Jan. 6, 1976, Resist process; Diana Jean Bendz, et al., 43Ø/313; 156/651; 427/96, 259; 43Ø/312, 314, 315, 316, 318, 323, 324,

DIG.164; 156/643, 644, 646; 437/195, 203, 915, 978

19. 4,840,654, Jun. 20, 1989, Method for making multi-layer and pin grid arrays; Michael J. Pryor, 65/18.1, 42, 59.5; 156/624, 644, 663

20. 4,795,512, Jan. 3, 1989, Method of manufacturing a multilayer ceramic body; Seiichi Nakatani, et al., 156/89; 427/96

21. 4,771,013, Sep. 13, 1988, Process of making a double heterojunction 3-D I.sup.2 L bipolar transistor with a Si/Ge superlattice; Patrick A. Curran,

437/31; 148/DIG.11, DIG.12, DIG.142, DIG.147, DIG.160, DIG.164, DIG.169; 156/613, 614; 357/34, 56, 92; 437/55, 106, 110, 111, 131, 174, 200

22. 4,750,092, Jun. 7, 1988, Interconnection package suitable for electronic devices and methods for producing same; William E. Werther, 361/400; 29/830; 156/629; 361/386 [IMAGE AVAILABLE]

23. 4,737,236, Apr. 12, 1988, Method of making microwave integrated circuits; Richard J. Perko, et al., 156/644; 29/846; 156/633, 651, 654, 659.1, 663, 901, 902

24. 4,722,914, Feb. 2, 1988, Method of making a high density IC module assembly; James E. Drye, et al., 437/213; 29/740; 156/644, 662; 174/52.2; 357/73; 437/981, 982 [IMAGE AVAILABLE]

25. 4,717,681, Jan. 5, 1988, Method of making a heterojunction bipolar

transistor with SIPOS; Patrick A. Curran, 437/31; 156/614; 357/16, 34, 55, 59, 60, 67; 437/68, 106, 126, 196, 203

26. 4,708,904, Nov. 24, 1987, Semiconductor device and a method of manufacturing the same; Masahiro Shimizu, et al., 428/209; 156/656, 657; 204/192.34; 427/96; 428/901; 430/396; 437/192, 200, 946

27. 4,701,363, Oct. 20, 1987, Process for manufacturing bumped tape for tape automated bonding and the product produced thereby; Larry J. Barber, 428/137; 29/827; 156/630, 634, 644, 656, 659.1, 661.1, 902; 357/70; 361/421; 428/156, 571, 573; 430/318 [IMAGE AVAILABLE]

28. 4,663,186, May 5, 1987, Screenable paste for use as a barrier layer on a substrate during maskless cladding; Richard F. Indyk, et al., 427/560; 29/846; 106/316; 156/645, 656, 904; 204/192.15; 427/96, 99, 259, 264, 266


29. 4,654,113, Mar. 31, 1987, Process for fabricating a semiconductor device; Takahiro Tuchiya, et al., 156/643, 644, 646, 653, 657, 659.1, 661.1, 668, 904; 437/186, 187, 191

30. 4,604,791, Aug. 12, 1986, Method for producing multi-layer, thin-film, flexible silicon alloy photovoltaic cells; William J. Todorof, 437/4; 148/557; 156/608, DIG.88; 264/332; 437/248

31. 4,419,809, Dec. 13, 1983, Fabrication process of sub-micrometer channel length MOSFETs; Jacob Riseman, et al., 437/41; 156/654; 357/23.3, 23.9; 437/27, 44, 70, 193, 200, 201, 931

32. 4,400,865, Aug. 30, 1983, Self-aligned metal process for integrated circuit metallization; George R. Goth, et al., 437/31; 156/643, 656; 357/34, 36, 59; 437/33, 39, 69, 194, 195, 203, 931

33. 4,396,457, Aug. 2, 19[redacted], Method of making bumped-[redacted]am tape; Frank C.

Bakenmaas, 437/183; 156/[redacted]

contact; Madhav Datta, et al., 29/884; 156/664; 204/129.65; 439/74 [IMAGE AVAILABLE]

5. 5,104,480, Apr. 14, 1992, Direct patterning of metals over a thermally inefficient surface using a laser; Robert J. Wojnarowski, et al., 156/643, 656; 219/121.69 [IMAGE AVAILABLE]

6. 5,024,883, Jun. 18, 1991, Electronic packaging of components

incorporating a ceramic-glass-metal composite; Narendra N. SinghDeo, et al., 428/323; 156/89; 361/403, 411; 428/328, 426, 428, 432, 433, 688, 901 [IMAGE AVAILABLE]

7. 5,000,113, Mar. 19, 1991, Thermal CVD/PECVD reactor and use for thermal chemical vapor deposition of silicon dioxide and in-situ multi-step planarized process; David N. Wang, et al., 118/723, 715, 725, 729; 156/345; 204/298.01, 298.07, 298.09, 298.23 [IMAGE AVAILABLE]

8. 4,997,517, Mar. 5, 1991, Multi-metal layer interconnect tape for tape automated bonding; Arvind Parthasarathi, 156/630; 29/827; 156/634, 644, 656, 659.1, 901; 437/220 [IMAGE AVAILABLE]

9. 4,970,107, Nov. 13, 1990, Composite article comprising a copper element and a process for producing it; Haruo Akahoshi, et al., 428/209; 156/60; 427/96; 428/409, 457, 901; 430/311 [IMAGE AVAILABLE]


10. 4,970,106, Nov. 13, 1990, Thin film multilayer laminate interconnection board; Thomas H. DiStefano, et al., 428/209; 156/634, 656, 902; 428/901 [IMAGE AVAILABLE]

11. 4,937,094, Jun. 26, 1990, Method of creating a high flux of activated species for reaction with a remotely located substrate; Joachim Doehler, et al., 427/574; 156/643, 646; 204/192.1; 427/294, 569, 575, 578 [IMAGE AVAILABLE]

12. 4,933,045, Jun. 12, 1990, Thin film multilayer laminate interconnection board assembly method; Thomas H. DiStefano, et al., 156/630; 29/852; 156/634, 643, 644, 645, 656, 659.1, 668, 902 [IMAGE AVAILABLE]

13. 4,872,947, Oct. 10, 1989, CVD of silicon oxide using TEOS decomposition

and in-situ planarization process; David N. Wang, et al., 156/643; 118/50.1, 620, 728; 156/345, 646, 653, 657; 204/192.12, 192.37, 298.33, 298.35; 427/248.1, 294, 574, 585; 437/235, 238

14. 4,871,595, Oct. 3, 1989, Lyotropic liquid crystalline oriented polymer substrate for printed wire board; Richard W. Lusignea, et al., 428/1; 156/150, 151, 330, 330.9; 174/256; 427/98; 428/901, 910; 525/903; 528/373; 548/152 [IMAGE AVAILABLE]

15. 4,863,683, Sep. 5, 1989, Conductor paste and method of manufacturing a multilayered ceramic body using the paste; Seiichi Nakatani, et al., 419/10; 156/89; 252/512, 513, 518, 519; 419/19, 53, 54, 57, 58 [IMAGE AVAILABLE]

16. 4,857,143, Aug. 15, 1989, Wet etching of cured polyimide; John J. Glenning, et al., 156/668, 655, 659.1; 252/79.5


17. 4,846,929, Jul. 11, 1989, Wet etching of thermally or chemically cured polyimide; Steven L. Bard, et al., 156/630, 644, 651, 655, 656, 659.1, 661.1, 668; 252/79.2, 79.5; 427/307

18. 4,840,923, Jun. 20, 1989, Simultaneous multiple level [redacted] process; Denis S. Simms, et al., 437/189; 148/DIG. 20

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=> s l18 and l21
L22 50 L18 AND L21

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1. 5,116,459, May 26, 1992, Processes for electrically conductive decals filled with organic insulator material; Mark R. Kordus, et al., 156/631, 634, 652, 656, 659.1, 661.1, 901 [IMAGE AVAILABLE]

2. 5,112,448, May 12, 1992, Self-aligned process for fabrication of
17 DEC 92 10:41:42 U.S. Patent & Trademark Office P0019
interconnect structures in semiconductor applications; Kishore K. Chakravorty, 205/118; 156/643, 652, 659.1; 205/182, 223, 224, 917; 437/192, 228 [IMAGE AVAILABLE]

3. 5,108,541, Apr. 28, 1992, Processes for electrically conductive decals filled with inorganic insulator material; Mark S. Schneider, et al., 156/631, 634, 652, 656, 661.1, 901 [IMAGE AVAILABLE]

34. 4,494,136, Jan. 15, 1985, Semiconductor device having an amorphous metal layer contact; John H. Perezko, et al., 357/67, 2, 68, 71

35. 4,404,059, Sep. 13, 1983, Process for manufacturing panels to be used in microelectronic systems; Vladimir I. Livshits, et al., 156/629; 29/846; 156/151, 630, 634, 651, 656, 902; 174/253; 205/125 [IMAGE AVAILABLE]



36. 4,272,722, Jun. 9, 1981, Determination of electric current flow patterns; Armando S. Cammarano, et al., 324/76R, 71.1

37. 4,260,428, Apr. 7, 1981, Photovoltaic cell; Pradip K. Roy, 136/260; 205/162, 164, 178, 183; 357/30; 427/74; 437/5

38. 4,022,931, May 10, 1977, Process for making semiconductor device; James R. Black, et al., 437/187; 156/654, 655; 357/65, 67, 68; 437/182, 188, 199

39. 3,617,816, Nov. 2, 1971, COMPOSITE METALLURGY STRIPE FOR SEMICONDUCTOR DEVICES; Jacob Riseman, et al., 361/160; 338/13, 17, 22R; 357/35, 67, 68, 71, 73, 85 [IMAGE AVAILABLE]



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=> s semiconductor
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L15          973 L13 AND L14

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17. 4,981,103, Jan. 1, 1991, Apparatus for forming a metal thin film utilizing temperature controlling means; Atsushi Sekiguchi, et al., 118/725, 724 [IMAGE AVAILABLE]

18. 4,980,705, Dec. 25, 1990, Print recording head; Eiichi Akutsu, et al., 346/155, 139C [IMAGE AVAILABLE]

19. 4,970,574, Nov. 13, 1990, Electromigrationproof structure for multilayer wiring on a semiconductor device; Kinji Tsunenari, 357/71, 65, 68 [IMAGE AVAILABLE]

20. 4,963,423, Oct. 16, 1990, Method for forming a thin film and apparatus of forming a metal thin film utilizing temperature controlling means; Atsushi Sekiguchi, et al., 428/209; 156/610, 614; 174/250; 361/397; 427/58, 96, 99, 372.2; 428/428, 457, 688, 689, 901 [IMAGE AVAILABLE]


21. 4,962,060, Oct. 9, 1990, Making a high speed interconnect system with refractory non-dogbone contacts and an active electromigration suppression mechanism; Jack Sliwa, et al., 437/192; 357/67; 428/651 [IMAGE AVAILABLE]

22. 4,922,322, May 1, 1990, Bump structure for reflow bonding of IC devices; Ranjan J. Mathew, 357/69; 228/123; 357/71 [IMAGE AVAILABLE]

23. 4,847,674, Jul. 11, 1989, High speed interconnect system with refractory non-dogbone contacts and an active electromigration suppression mechanism; Jack Sliwa, et al., 357/67, 23.2, 23.3; 361/411; 428/627 [IMAGE AVAILABLE]

24. 4,843,453, Jun. 27, 1989, Metal contacts and interconnections for VLSI devices; Robert C. Hooper, et al., 357/71, 65, 68; 427/305

25. 4,842,891, Jun. 27, 1989, Method of forming a copper film by chemical

vapor deposition; Hiroshi Miyazaki, et al., 427/569, 252, 584, 585; 437/245

26. 4,742,014, May 3, 1988, Method of making metal contacts and interconnections for VLSI devices with copper as a primary conductor; Robert C. Hooper, et al., 437/192, 198, 200, 203

27. 4,687,552, Aug. 18, 1987, Rhodium capped gold IC metallization; Stephen R. Early, et al., 205/125

28. 4,682,964, Jul. 28, 1987, Ionization detector; Douglas S. Steele, et al., 445/28; 250/385.1; 445/58

29. 4,648,175, Mar. 10, 1987, Use of selectively deposited tungsten for contact formation and shunting metallization; Werner A. Metz, Jr., et al., 437/192; 357/2, 23.1, 23.9, 42, 59, 71; 437/193, 245


30. 4,619,887, Oct. 28, 1986, Method of plating an interconnect metal onto a metal in VLSI devices; Robert C. Hooper, et al., 430/313; 156/642; 205/125; 430/314, 315, 316, 317, 318, 319

31. 4,613,314, Sep. 23, 1986, Ionization detector; Douglas S. Steele, 445/28; 156/645; 445/35, 59

32. 4,613,313, Sep. 23, 1986, Ionization detector; Douglas S. Steele, 445/28; 29/446; 156/634; 250/374, 385.1; 445/35, 59

33. 4,570,071, Feb. 11, 1986, Ionization detector; Theodore W. Sippel, et al., 250/374, 385.1

1. 5,171,713, Dec. 15, 1992, Process for forming planarized, air-bridge interconnects on a semiconductor substrate; James A. Matthews, 437/189; 148/DIG.20; 257/750; 437/183, 195, 228 [IMAGE AVAILABLE]

2. 5,162,690, Nov. 10, 1992, Surface acoustic wave device; Hideharu Ieki, et al., 310/313R, 313B, 313C, 313D, 363, 364 [IMAGE AVAILABLE]

3. 5,152,864, Oct. 6, 1992, Method of manufacturing surface acoustic wave device; Hideharu Ieki, et al., 156/610; 310/313B, 313R; 427/100, 126.4 [IMAGE AVAILABLE]



4. 5,151,168, Sep. 29, 1992, Process for metallizing integrated circuits with electrolytically-deposited copper; Terry L. Gilton, et al., 205/123, 135 [IMAGE AVAILABLE]

5. 5,150,193, Sep. 22, 1992, Resin-encapsulated semiconductor device having a particular mounting structure; Toshihiro Yasuhara, et al., 357/70, 72 [IMAGE AVAILABLE]

6. 5,134,083, Jul. 28, 1992, Method of forming self-aligned contacts in a semiconductor process; James A. Matthews, 437/40; 148/DIG.19; 437/31, 56, 193, 200, 228 [IMAGE AVAILABLE]

7. 5,132,237, Jul. 21, 1992, Planarization method for fabricating high density semiconductor devices; James A. Matthews, 437/40, 41, 50, 67, 193, 228 [IMAGE AVAILABLE]



8. 5,130,779, Jul. 14, 1992, Solder mass having conductive encapsulating arrangement; Birendra N. Agarwala, et al., 357/67, 68, 71 [IMAGE AVAILABLE]

9. 5,112,761, May 12, 1992, BiCMOS process utilizing planarization technique; James A. Matthews, 437/31; 357/43; 437/34, 44, 50, 57, 162, 193, 200, 228 [IMAGE AVAILABLE]

10. 5,108,945, Apr. 28, 1992, Process for fabricating polysilicon resistors and interconnects; James A. Matthews, 437/60; 148/DIG.136; 437/41, 59, 193, 918 [IMAGE AVAILABLE]

11. 5,107,283, Apr. 21, 1992, Electrostatic recording head with improved alignment of recording electrodes; Noboru Ueno, et al., 346/155, 139C [IMAGE AVAILABLE]

12. 5,080,763, Jan. 14, 1992, Method of forming conductor lines of a



semiconductor device; Aiichirou Baigetsu, 205/95, 125, 266 [IMAGE AVAILABLE]

13. 5,070,591, Dec. 10, 1991, Method for clad-coating refractory and transition metals and ceramic particles; Nathaniel R. Quick, et al., 29/527.4; 75/342; 164/91; 419/2, 12, 13, 14, 19, 23, 28, 47 [IMAGE AVAILABLE]

14. 5,061,985, Oct. 29, 1991, Semiconductor integrated circuit device and process for producing the same; Hideo Meguro, et al., 357/68, 71 [IMAGE AVAILABLE]

15. 5,019,891, May 28, 1991, Semiconductor device and method of fabricating the same; Jin Onuki, et al., 357/70, 65, 67, 71, 72; 428/620, 632, 634 [IMAGE AVAILABLE]

16. 5,010,252, Apr. 23, 1991, Ionization detector; Douglas S. Steele, 250/385.1, 374 [IMAGE AVAILABLE]

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1. 5,171,713, Dec. 15, 1992, Process for forming planarized, air-bridge interconnects on a semiconductor substrate; James A. Matthews, 437/189; 148/DIG.20; 257/750; 437/183, 195, 228 [IMAGE AVAILABLE]

2. 5,162,258, Nov. 10, 1992, Three metal personalization of application specific monolithic microwave integrated circuit; Zachary J. Lemnios, et al., 437/184; 257/296, 528; 437/47, 51, 60, 195, 919 [IMAGE AVAILABLE]

3. 5,134,083, Jul. 28, 1992, Method of forming self-aligned contacts in a semiconductor process; James A. Matthews, 437/40; 148/DIG.19; 437/31,
17 DEC 92 14:45:37 U.S. Patent & Trademark Office P0006
56, 193, 200, 228 [IMAGE AVAILABLE]

4. 5,132,237, Jul. 21, 1992, Planarization method for fabricating high density semiconductor devices; James A. Matthews, 437/40, 41, 50, 67, 193, 228 [IMAGE AVAILABLE]

5. 5,112,761, May 12, 1992, BiCMOS process utilizing planarization technique; James A. Matthews, 437/31; 357/43; 437/34, 44, 50, 57, 162, 193, 200, 228 [IMAGE AVAILABLE]

6. 5,108,945, Apr. 28, 1992, Process for fabricating polysilicon resistors and interconnects; James A. Matthews, 437/60; 148/DIG.136; 437/41, 59, 193, 918 [IMAGE AVAILABLE]

7. 5,081,067, Jan. 14, 1992, Ceramic package type semiconductor device and method of assembling the same; Nobutaka Shimizu, et al., 437/209; 357/74, 80; 361/381; 437/215, 216, 217, 218 [IMAGE AVAILABLE]
17 DEC 92 14:45:48 U.S. Patent & Trademark Office P0007

8. 5,055,427, Oct. 8, 1991, Process of forming self-aligned interconnects for semiconductor devices; Jacob D. Haskell, 437/203, 46, 186, 187, 228 [IMAGE AVAILABLE]

9. 5,028,555, Jul. 2, 1991, Self-aligned semiconductor devices; Jacob D. Haskell, 437/57; 148/DIG.50, DIG.141; 357/23.5, 23.9; 437/40, 41, 228, 233, 984 [IMAGE AVAILABLE]

10. 4,977,108, Dec. 11, 1990, Method of making self-aligned, planarized contacts for semiconductor devices; Jacob D. Haskell, 437/229; 148/DIG.50, DIG.141; 437/41, 56, 193, 228 [IMAGE AVAILABLE]

11. 4,868,014, Sep. 19, 1989, Method for forming thin film multi-layer structure member; Masahiro Kanai, et al., 427/248.1; 136/258; 427/255, 255.1, 255.2, 255.3, 255.7; 437/225
17 DEC 92 14:45:59 U.S. Patent & Trademark Office P0008

12. 4,842,897, Jun. 27, 1989, Method for forming deposited film; Eiji Takeuchi, et al., 427/255.2; 136/258; 156/646; 427/255, 255.3, 307, 309; 437/225, 228, 234

13. 4,801,474, Jan. 31, 1989, Method for forming thin film multi-layer structure member; Keisha Saitoh, et al., 427/248.1; 136/258; 427/255, 255.1, 255.2, 255.3, 255.7; 437/233, 234

14. 4,798,809, Jan. 17, 1989, Process for preparing photoelectromotive force member; Masaaki Hirooka, et al., 437/4; 136/258; 427/74; 437/100, 101

15. 4,772,570, Sep. 20, 1988, Method for producing an electronic device having a multi-layer structure; Masahiro Kanai, et al., 437/109; 136/258; 427/74, 574, 585; 437/4, 101



16. 4,771,015, Sep. 13, 1988, Method for producing an electronic device having a multi-layer structure; Masahiro Kanai, et al., 437/109; 136/258; 427/74, 574; 437/4, 101

17. 4,766,091, Aug. 23, 1988, Method for producing an electronic device having a multi-layer structure; Hirokazu Ohtoshi, et al., 437/108; 136/258; 204/157.4, 157.45; 427/74, 583; 430/128; 437/4, 100, 101, 109

18. 4,758,528, Jul. 19, 1988, Self-aligned metal process for integrated circuit metallization; George R. Goth, et al., 437/15; 357/34; 437/147, 228, 233, 238

19. 4,735,822, Apr. 5, 1988, Method for producing an electronic device having a multi-layer structure; Hirokazu Ohtoshi, et al., 427/582; 136/258; 427/74, 255.1, 255.2, 583; 437/4, 101



20. 4,708,904, Nov. 24, 1987, Semiconductor device and a method of manufacturing the same; Masahiro Shimizu, et al., 428/209; 156/656, 657; 204/192.34; 427/96; 428/901; 430/396; 437/192, 200, 946

21. 4,654,224, Mar. 31, 1987, Method of manufacturing a thermoelectric element; David Allred, et al., 427/456; 156/646; 204/192.15; 205/181, 183, 186, 187, 191, 192, 193, 227, 917; 427/58, 124, 250; 437/190

22. 4,609,567, Sep. 2, 1986, High efficiency stable CdS-Cu.sub.2 S solar cells manufacturing process using thick film methodology; Ottilia F. Toth, et al., 427/74; 136/258, 260, 265; 437/4, 965

23. 4,400,865, Aug. 30, 1983, Self-aligned metal process for integrated circuit metallization; George R. Goth, et al., 437/31; 156/643, 656; 357/34, 36, 59; 437/33, 39, 69, 194, 195, 203,



931

24. 4,322,883, Apr. 6, 1982, Self-aligned metal process for integrated injection logic integrated circuits; Shakir A. Abbas, et al., 437/32; 148/DIG.131; 156/628, 643, 653, 657; 357/54, 59, 92; 437/55, 69, 187, 228, 229, 917, 924, 931, 967, 968, 978, 984

25. 3,771,219, Nov. 13, 1973, METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE; Takateru Tuzi, et al., 437/182; 357/54, 69

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L6 223 S L3 AND L5
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L8 135 S L6 AND
L9 25 S L8 AND 437/CLAS

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1. 5,047,114, Sep. 10, 1991, Process for the production of metal clad

thermoplastic base materials and printed circuits on thermoplastic base materials; David C. Frisch, et al., 156/630, 308.2, 309.6, 309.9, 322, 902 [IMAGE AVAILABLE]

2. 4,937,094, Jun. 26, 1990, Method of creating a high flux of activated species for reaction with a remotely located substrate; Joachim Doehler, et al., 427/574; 156/643, 646; 204/192.1; 427/294, 569, 575, 578 [IMAGE AVAILABLE]

3. 4,913,768, Apr. 3, 1990, Process for producing electrical conductor boards; Gerhard D. Wolf, et al., 156/645; 29/852; 156/656, 659.1, 666, 902; 427/97, 98 [IMAGE AVAILABLE]

4. 4,845,311, Jul. 4, 1989, Flexible coaxial cable apparatus and method; Christopher M. Schreiber, et al., 174/36; 29/828; 156/47, 55; 174/103, 104, 117FF; 333/1, 243 [IMAGE AVAILABLE]


5. 4,842,897, Jun. 27, 1989, Method for forming deposited film; Eiji Takeuchi, et al., 427/255.2; 136/258; 156/646; 427/255, 255.3, 307, 309; 437/225, 228, 234

6. 4,840,654, Jun. 20, 1989, Method for making multi-layer and pin grid arrays; Michael J. Pryor, 65/18.1, 42, 59.5; 156/624, 644, 663

7. 4,790,902, Dec. 13, 1988, Method of producing conductor circuit boards; Tatsuo Wada, et al., 156/630; 29/848; 156/151, 153, 233, 236, 240, 249, 631, 634, 645, 650, 656, 659.1, 666, 902; 205/125

8. 4,708,904, Nov. 24, 1987, Semiconductor device and a method of manufacturing the same; Masahiro Shimizu, et al., 428/209; 156/656, 657; 204/192.34; 427/96; 428/901; 430/396; 437/192, 200, 946


9. 4,654,224, Mar. 31, 1987, Method of manufacturing a thermoelectric element; David Allred, et al., 427/456; 156/646; 204/192.15; 205/181, 183, 186, 187, 191, 192, 193, 227, 917; 427/58, 124, 250; 437/190

10. 4,597,828, Jul. 1, 1986, Method of manufacturing printed circuit boards; Jehane Tadros, 156/643, 646, 655, 656, 668, 902; 204/192.15, 192.3; 427/96

11. 4,424,095, Jan. 3, 1984, Radiation stress relieving of polymer articles; David C. Frisch, et al., 156/629; 29/852; 156/83, 272.2, 280, 630, 643, 645, 668, 902; 174/256; 264/22; 427/97, 307, 553, 557, 558; 428/131, 137, 901 [IMAGE AVAILABLE]

12. 4,400,865, Aug. 30, 1983, Self-aligned metal process for integrated circuit metallization; George R. Goth, et al., 437/31; 156/643, 656; 357/34, 36, 59; 437/33, 39, 69, 194, 195, 203, 931


13. 4,339,303, Jul. 13, 1982, Radiation stress relieving of sulfone polymer articles; David C. Frisch, et al., 156/629; 29/852; 156/83, 272.2, 280, 630, 643, 645, 668, 902; 174/258; 264/22; 427/97, 307, 544; 428/131, 137, 901 [IMAGE AVAILABLE]

14. 4,330,353, May 18, 1982, Method to improve wetting of peelable adhesive structures; Go Kunimoto, et al., 156/314; 40/311; 156/315, 322, 324.4, 330, 334; 215/347; 428/458, 460, 461, 463

15. 4,322,883, Apr. 6, 1982, Self-aligned metal process for integrated injection logic integrated circuits; Shakir A. Abbas, et al., 437/32; 148/DIG.131; 156/628, 643, 653, 657; 357/54, 59, 92; 437/55, 69, 187, 228, 229, 917, 924, 931, 967, 968, 978, 984

16. 4,253,907, Mar. 3, 1981, Anisotropic plasma etching; Peter D. Parry, et

al., 156/643, 646, 656, 657, 659.1; 204/192.32, 298.33, 298.34; 219/121.41, 121.42, 121.43; 422/186.05, 186.29 [IMAGE AVAILABLE]

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        346305 LAYER
         11583 MULTI-LAYER
                 (MULTI(W)LAYER)
         27692 PLATING
L11         44 MULTI-LAYER(4A)PLATING

=> s multi-layer(2a)plating
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        346305 LAYER
17:00:42 14:50:34           U.S. Patent & Trademark Office          P0018
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         27692 PLATING
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1. 5,151,167, Sep. 29, 1992, Coins coated with nickel, copper and nickel and process for making such coins; Hieu C. Truong, et al., 205/102; 72/46; 205/149, 181, 217, 222, 227 [IMAGE AVAILABLE]

2. 5,139,886, Aug. 18, 1992, Coins coated with nickel, copper and nickel; Hieu Truong, et al., 428/577; 40/27.5; 428/675, 679 [IMAGE AVAILABLE]

3. 5,092,036, Mar. 3, 1992, Ultra-tall indium or alloy bump array for IR detector hybrids and micro-electronics; William C. Hu, et al., 29/854; 250/332, 338.1, 349; 357/68 [IMAGE AVAILABLE]


4. 4,992,154, Feb. 12, 1991, Brush for electrolytic treatment; Yoshiaki Ida, et al., 204/224R, 224M, 271 [IMAGE AVAILABLE]

5. 4,975,337, Dec. 4, 1990, Multi-layer corrosion resistant coating for fasteners and method of making; Jacob Hyner, et al., 428/648; 205/176, 177, 180, 181, 196; 427/406; 428/658, 667, 674, 675, 679, 935 [IMAGE AVAILABLE]

6. 4,933,010, Jun. 12, 1990, Sensitizing activator composition for chemical plating; Kiyoshi Okabayashi, 106/1.11 [IMAGE AVAILABLE]

7. 4,842,961, Jun. 27, 1989, Alternate electrolytic/electroless-layered lid for electronics package; Thomas J. Basile, et al., 428/672; 174/52.4; 205/181, 917; 427/125, 305, 405, 438; 428/679, 680, 935, 936; 437/221 [IMAGE AVAILABLE]

8. 4,548,872, Oct. 22, 1985, Protection process of flat rolled steel

sections by means of multi-layer electrolytic Plating[illegible] particularly aggressive environments; Carlo Lavezzari, 428/633; 205/130, 156, 179, 183, 206, 224; 428/659, 667

9. 4,520,077, May 28, 1985, Process for the protection of galvanized steel rolled sections with a two-layer chromium-chromate coating; Carlo Lavezzari, 428/632; 205/130, 137, 158, 179, 284, 319

10. 4,331,258, May 25, 1982, Sealing cover for an hermetically sealed container; Gary I. Geschwind, 220/359; 174/52.3, 52.4, 66; 220/200 [IMAGE AVAILABLE]

11. 4,329,402, May 11, 1982, Micro-throwing alloy undercoatings and method for improving corrosion resistance; Jacob Hyner, et al., 428/621; 205/95, 176, 194, 196, 197; 411/902; 427/405; 428/657, 658, 659, 679, 926, 935



12. 4,326,911, Apr. 27, 1982, Reactive ion etching of III-V compounds including InP, GaAs-InP and GaAlAs; Richard E. Howard, et al., 156/643; 148/DIG.105; 156/646, 655, 662; 204/192.32; 252/79.1

13. 4,296,424, Oct. 20, 1981, Compound semiconductor device having a semiconductor-converted conductive region; Ichiro Shibasaki, et al., 357/1; 174/257, 260; 357/2, 65, 67, 68 [IMAGE AVAILABLE]

14. 4,188,459, Feb. 12, 1980, Corrosion resistant plating and method utilizing alloys having micro-throwing power; Jacob Hyner, et al., 428/648; 205/176; 411/902; 427/405, 406; 428/658, 659, 667, 674, 675, 678, 679

15. 4,143,210, Mar. 6, 1979, Multi-layer Plating for improved corrosion resistance; Jacob Hyner, et al., 428/646, 648, 657, 659, 666, 668

16. 4,120,439, Oct. 17, 1978, Method for welding by explosion of powder material on a firm surface; Per Ingemar Persson, 228/107; 29/421.2



17. 4,082,621, Apr. 4, 1978, Plating method with lead or tin sublayer; Nicholas J. Spiliotis, et al., 205/113, 176, 178, 180, 286; 428/626, 645, 646, 648

18. 3,827,004, Jul. 30, 1974, CIRCUIT BOARD PIN; Milike Vanden Heuvel, et al., 439/873; 174/262; 411/452; 439/876 [IMAGE AVAILABLE]

19. 3,731,630, May 8, 1973, HIGH-EXPLOSIVE ARMOR-PIERCING SHELL; Kurt Muller, 102/518; 29/1.23; 89/36.02; 102/522 [IMAGE AVAILABLE]

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L3           2366 S L1 AND L2
L4          17354 S ANNEALING
L5          24896 S ANNEAL###
L6            223 S L3 AND L5
L7         506816 S MIX#####
L8            135 S L6 AND L7
L9             25 S L8 AND 437/CLAS
L10            16 S L8 AND 156/CLAS
L11            44 S MULTI-LAYER(4A)PLATING
L12            19 S MULTI-LAYER(2A)PLATING

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         15824 437/CLAS
L13          1 L11 AND 437/CLAS
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1. 4,842,961, Jun. 27, 1989, Alternate electrolytic/electroless-layered lid for electronics package; Thomas J. Basile, et al., 428/672; 174/52.4; 205/181, 917; 427/125, 305, 405, 438; 428/679, 680, 935, 936; 437/221 [IMAGE AVAILABLE]

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L14          2 L11 AND 156/CLAS

=> d 1-2

1. 4,401,499, Aug. 30, 1983, Crosslinked resin of epoxy compound and isocyanate and process for producing same; Shoroku Kaneko, et al., 156/307.3, 307.1; 427/386; 525/113, 407
17 DEC 92 14:52:32 U.S. Patent & Trademark Office P0025

2. 4,326,911, Apr. 27, 1982, Reactive ion etching of III-V compounds including InP, GaAs-InP and GaAlAs; Richard E. Howard, et al., 156/643; 148/DIG.105; 156/648, 655, 662; 204/192.32; 252/79.1

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1. 5,132,248, Jul. 21, 1992, Direct write with microelectronic circuit fabrication; Timothy Drummond, et al., 437/173; 427/96; 437/174, 935 [IMAGE AVAILABLE]

2. 5,Ø45,4Ø9, Sep. 3, 1991, Process for making thin film solar cell; Chris Eberspacher, et al., 428/62Ø; 136/264, 265; 148/33; 423/5Ø8; 427/76; 437/5, 232 [IMAGE AVAILABLE]

3. 4,927,5Ø5, May 22, 199Ø, Metallization scheme providing adhesion and barrier properties; Ravinder K. Sharma, et al., 2Ø5/123; 2Ø4/192.25, 192.3; 2Ø5/135; 357/71; 428/62Ø; 437/192 [IMAGE AVAILABLE]

4. 4,915,745, Apr. 1Ø, 199Ø, Thin film solar cell and method of making; Gary A. Pollock, et al., 136/265, 26Ø, 264; 357/3Ø; 427/76; 437/5 [IMAGE AVAILABLE]
17 DEC 92 14:Ø2:14 U.S. Patent & Trademark Office P0014

5. 4,88Ø,7Ø8, Nov. 14, 1989, Metallization scheme providing adhesion and barrier properties; Ravinder K. Sharma, et al., 428/62Ø; 156/652, 664; 428/623, 626; 437/192, 194, 246

6. 4,837,182, Jun. 6, 1989, Method of producing sheets of crystalline material; Carl O. Bozler, et al., 437/82; 148/DIG.26, DIG.48, DIG.54, DIG.9Ø, DIG.135; 156/DIG.88; 437/86, 89, 1Ø8, 174, 962, 966, 974

7. 4,816,42Ø, Mar. 28, 1989, Method of producing tandem solar cell devices from sheets of crystalline material; Carl O. Bozler, et al., 437/2; 136/249; 148/DIG.54; 156/DIG.88; 437/5, 966

8. 4,727,Ø47, Feb. 23, 1988, Method of producing sheets of crystalline material; Carl O. Bozler, et al., 437/89; 156/612, DIG.84, DIG.88; 357/4; 437/2, 82, 86, 249, 927, 962, 966, 974
17 DEC 92 14:Ø2:25 U.S. Patent & Trademark Office P0015

9. 4,594,77Ø, Jun. 17, 1986, Method of making semiconductor casing; Sheldon H. Butt, 437/219; 174/52.4; 437/22Ø [IMAGE AVAILABLE]

1Ø. 4,581,1Ø8, Apr. 8, 1986, Process of forming a compound semiconductive material; Vijay K. Kapur, et al., 2Ø5/17Ø; 136/26Ø, 262, 264, 265; 2Ø4/86; 2Ø5/182, 194, 229; 437/5

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L10             Ø  S L8 AND L9

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L11            8  L4 AND L9

=> d 1-8

1.  4,97Ø,123, Nov. 13, 199Ø, Isotropically reinforced net-shape
microcomposites; Horst Witzke, et al., 428/545; 156/3Ø7.7; 264/29.2,
29.6, 82, 135, 137, 257, 299; 423/447.2, 447.3, 447.5; 427/249, 25Ø; 428/283,
288, 289, 29Ø, 4Ø8, 413, 418, 469, 539.5, 549, 689, 699; 5Ø1/95, 99 [IMAGE
AVAILABLE]
17 DEC 92 14:ØØ:2Ø            U.S. Patent & Trademark Office            PØØ11

2.  4,88Ø,7Ø8, Nov. 14, 1989, Metallization scheme providing adhesion and
barrier properties; Ravinder K. Sharma, et al., 428/62Ø; 156/652,
664; 428/623, 626; 437/192, 194, 246

3.  4,837,182, Jun. 6, 1989, Method of producing sheets of crystalline
material; Carl O. Bozler, et al., 437/82; 148/DIG.26, DIG.4B, DIG.54, DIG.9Ø,
DIG.135; 156/DIG.88; 437/86, 89, 1Ø8, 174, 962, 966, 974

4.  4,816,42Ø, Mar. 28, 1989, Method of producing tandem solar cell devices
from sheets of crystalline material; Carl O. Bozler, et al., 437/2; 136/249;
148/DIG.54; 156/DIG.88; 437/5, 966

5.  4,727,Ø47, Feb. 23, 1988, Method of producing sheets of crystalline
material; Carl O. Bozler, et al., 437/89; 156/612, DIG.84,
DIG.88; 357/4; 437/2, 82, 86, 249, 927, 962, 966, 974

17 DEC 92 14:ØØ:31            U.S. Patent & Trademark Office            PØØ12
6.  4,645,718, Feb. 24, 1987, Ferrous substrate with rubber adherent metal
coating and method of making the same; Paul Dambre, 428/625; 57/9Ø2; 152/451,
527, 556, 565; 156/124, 91Ø; 2Ø5/141, 149, 151, 155, 222, 228;
428/677, 684

7.  4,518,457, May 21, 1985, Raney alloy coated cathode for chlor-alkali
cells; Thomas J. Gray, 148/527; 156/656, 664, 665; 427/123, 352,
376.8, 377, 4Ø5, 436; 5Ø2/1Ø1

8.  4,37Ø,361, Jan. 25, 1983, Process of forming Raney alloy coated cathode
for chlor-alkali cells; Thomas J. Gray, 148/527; 156/656, 664;
2Ø4/29ØR, 293; 427/123, 352, 376.8, 377, 4Ø5, 436; 5Ø2/3Ø1, 314, 315

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L12            1Ø  L5 AND L9
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1. 5,171,713, Dec. 15, 1992, Process for forming planarized, air-bridge interconnects on a semiconductor substrate; James A. Matthews, 437/189; 148/DIG.20; 257/750; 437/183, 195, 228 [IMAGE AVAILABLE]

2. 5,134,083, Jul. 28, 1992, Method of forming self-aligned contacts in a semiconductor process; James A. Matthews, 437/40; 148/DIG.19; 437/31, 56, 193, 200, 228 [IMAGE AVAILABLE]
17 DEC 92 13:58:16 U.S. Patent & Trademark Office P0006

3. 5,132,237, Jul. 21, 1992, Planarization method for fabricating high density semiconductor devices; James A. Matthews, 437/40, 41, 50, 67, 193, 228 [IMAGE AVAILABLE]

4. 5,112,761, May 12, 1992, BiCMOS process utilizing planarization technique; James A. Matthews, 437/31; 357/43; 437/34, 44, 50, 57, 162, 193, 200, 228 [IMAGE AVAILABLE]

5. 5,108,945, Apr. 28, 1992, Process for fabricating polysilicon resistors and interconnects; James A. Matthews, 437/60; 148/DIG.136; 437/41, 59, 193, 918 [IMAGE AVAILABLE]

6. 5,075,756, Dec. 24, 1991, Low resistance contacts to semiconductor materials; Ranjan Dutta, 357/67, 65; 437/180, 184 [IMAGE AVAILABLE]

7. 5,011,792, Apr. 30, 1991, Method of making ohmic resistance WSb, contacts
17 DEC 92 13:58:28 U.S. Patent & Trademark Office P0007
to III-V semiconductor materials; Ranjan Dutta, 437/184; 148/DIG.20; 357/65, 67; 437/192 [IMAGE AVAILABLE]

8. 4,954,214, Sep. 4, 1990, Method for making interconnect structures for VLSI devices; Vu Quoc Ho, 156/628, 652, 653, 655, 656, 657; 437/228 [IMAGE AVAILABLE]

9. 4,742,014, May 3, 1988, Method of making metal contacts and interconnections for VLSI devices with copper as a primary conductor; Robert C. Hooper, et al., 437/192, 198, 200, 203

10. 4,648,175, Mar. 10, 1987, Use of selectively deposited tungsten for contact formation and shunting metallization; Werner A. Metz, Jr., et al., 437/192; 357/2, 23.1, 23.9, 42, 59, 71; 437/193, 245

11. 4,310,568, Jan. 12, 1982, Method of fabricating improved Schottky
17 DEC 92 13:58:39 U.S. Patent & Trademark Office P0008
barrier contacts; James K. Howard, et al., 437/175; 204/192.15

12. 4,260,428, Apr. 7, 1981, Photovoltaic cell; Pradip K. Roy, 136/260; 205/162, 164, 178, 183; 357/30; 427/74; 437/5

13. 4,022,931, May 10, 1977, Process for making semiconductor device; James R. Black, et al., 437/187; 156/654, 655; 357/65, 67, 68; 437/182, 188, 199

=> s inter(w)diffusion or inter-diffusion or interdiffusion
56435 INTER
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17 DEC 92 13:59:25 U.S. Patent & Trademark Office P0009
(INTER(W)DIFFUSION)

Search plating and 437/195

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1. 5,200,300, Apr. 6, 1993, Methods for forming high density multi-chip carriers; Jacques Leibovitz, et al., 430/312; 428/137, 209; 430/311; 437/189, 195 [IMAGE AVAILABLE]

2. 5,198,389, Mar. 30, 1993, Method of metallizing contact holes in a semiconductor device; Andreas M. Th. P. van der Putten, et al., 437/190; 427/98; 437/192, 195, 230 [IMAGE AVAILABLE]

3. 5,196,377, Mar. 23, 1993, Method of fabricating silicon-based carriers; John J. Wagner, et al., 437/225, 195, 203, 974 [IMAGE AVAILABLE]

12 APR 93 13:58:40 U.S. Patent & Trademark Office P0064

4. 5,187,119, Feb. 16, 1993, Multichip module and integrated circuit substrates having planarized patterned surfaces; Jay M. Cech, et al., 437/187, 189, 195, 228 [IMAGE AVAILABLE]

5. 5,171,713, Dec. 15, 1992, Process for forming planarized, air-bridge interconnects on a semiconductor substrate; James A. Matthews, 437/189; 148/DIG.20; 257/750; 437/183, 195, 228 [IMAGE AVAILABLE]

6. 5,166,097, Nov. 24, 1992, Silicon wafers containing conductive feedthroughs; Minas H. Tanielian, 437/203, 195, 915 [IMAGE AVAILABLE]

7. 5,162,260, Nov. 10, 1992, Stacked solid via formation in integrated circuit systems; Jacques Leibovitz, et al., 437/195, 189, 192, 203, 228, 246, 978 [IMAGE AVAILABLE]

8. 5,162,258, Nov. 10, 1992, Three metal personalization of application specific monolithic microwave integrated circuit; Zachary J. Lemnios, et al.,

12 APR 93 13:58:51 U.S. Patent & Trademark Office P0065

437/184; 257/296, 528; 437/47, 51, 60, 195, 919 [IMAGE AVAILABLE]

9. 5,106,461, Apr. 21, 1992, High-density, multi-level interconnects, flex circuits, and tape for tab; David Volfson, et al., 205/125; 437/180, 195 [IMAGE AVAILABLE]

10. 5,098,860, Mar. 24, 1992, Method of fabricating high-density interconnect structures having tantalum/tantalum oxide layers; Kishore K. Chakravorty, et al., 437/195; 205/118, 122; 437/189, 192, 198, 230 [IMAGE AVAILABLE]

11. 5,071,518, Dec. 10, 1991, Method of making an electrical multilayer interconnect; Ju-Don T. Pan, 205/122, 135, 184, 187; 437/195 [IMAGE AVAILABLE]

12. 5,055,425, Oct. 8, 1991, Stacked solid via formation in integrated

12 APR 93 13:59:00 U.S. Patent & Trademark Office P0066

circuit systems; Jacques Leibovitz, et al., 437/195; 148/DIG.164; 156/643, 645, 650; 437/189, 203, 208, 228, 246, 915, 978 [IMAGE AVAILABLE]

13. 5,017,509, May 21, 1991, Stand-off transmission lines and method for making same; David B. Tuckerman, 437/182, 190, 195, 962 [IMAGE AVAILABLE]

14. 4,996,133, Feb. 26, 1991, Self-aligned tungsten-filled via process and via formed thereby; Jeffrey E. Brighton, et al., 430/313, 316, 317, 318; 437/192, 195, 228, 229 [IMAGE AVAILABLE]

15. 4,980,034, Dec. 25, 1990, High-density, multi-level interconnects, flex circuits, and tape for TAB; David Volfson, et al., 205/122; 437/180, 195 [IMAGE AVAILABLE]

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        950332 LOWER
        114496 CONDUCTOR
           493 LOWER CONDUCTOR
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L5           0 L4 AND LOWER CONDUCTOR

=> s plating(p)lower conductor
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=> s plating(p)lower conductor
         28407 PLATING
        950332 LOWER
        114496 CONDUCTOR
           493 LOWER CONDUCTOR
                 (LOWER(W)CONDUCTOR)
L6           9 PLATING(P)LOWER CONDUCTOR

=> d 1-9

1.  5,095,402, Mar. 10, 1992, Internally decoupled integrated circuit
package; Jorge M. Hernandez, et al., 361/306; 257/691, 724 [IMAGE AVAILABLE]

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12 APR 93 14:03:17              U.S. Patent & Trademark Office              P0072
2.  4,770,921, Sep. 13, 1988, Self-shielding multi-layer circuit boards;
Thomas P. Wacker, et al., 428/209; 174/250; 361/398, 402; 428/447, 546, 549,
551, 901 [IMAGE AVAILABLE]

3.  4,769,269, Sep. 6, 1988, Article containing conductive through-holes;
Daniel D. Johnson, et al., 428/131, 137, 209, 210, 901

4.  4,727,633, Mar. 1, 1988, Method of securing metallic members together;
Geoffrey C. Herrick, 228/122; 29/827, 840; 228/180.2, 254, 263.18, 263.21

5.  4,570,031, Feb. 11, 1986, High capacitance laminated buss and method of
manufacture; Kazuo Inoue, 174/72B; 29/854; 361/330 [IMAGE AVAILABLE]

6.  4,528,072, Jul. 9, 1985, Process for manufacturing hollow multilayer
printed wiring board; Keiji Kurosawa, et al., 29/830; 205/125; 427/96

7.  4,517,050, May 14, 1985, Process for forming conductive through-holes
12 APR 93 14:03:26              U.S. Patent & Trademark Office              P0073
through a dielectric layer; Daniel D. Johnson, et al., 156/643; 29/853, 882;
156/644, 645, 652, 902; 174/266; 427/97; 430/313, 317, 318 [IMAGE AVAILABLE]

8.  4,368,503, Jan. 11, 1983, Hollow multilayer printed wiring board; Keiji
Kurosawa, et al., 361/414; 174/263; 361/382, 385, 415 [IMAGE AVAILABLE]

9.  4,193,048, Mar. 11, 1980, Balun transformer; Orville K. Nyhus, 333/26,
246; 455/326

=> s polishing(p)carrier#
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        223289 CARRIER#
L7         564 POLISHING(P)CARRIER#

=> s 17(p)chip#
12 APR 93 14:05:17              U.S. Patent & Trademark Office              P0074
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1.  5,162,260, Nov. 10, 1992, Stacked solid via formation in integrated
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16. 4,943,539, Jul. 24, 1990, Process for making a multilayer metallization structure; Syd R. Wilson, et al., 437/195, 192, 228, 947 [IMAGE AVAILABLE]



17. 4,840,923, Jun. 20, 1989, Simultaneous multiple level interconnection process; Donis G. Flagello, et al., 437/189; 148/DIG.20, DIG.164; 156/643, 644, 646; 437/195, 203, 915, 978

18. 4,746,621, May 24, 1988, Planar tungsten interconnect; David C. Thomas, et al., 437/24, 37, 195, 200

19. 4,630,357, Dec. 23, 1986, Method for forming improved contacts between interconnect layers of an integrated circuit; Steven H. Rogers, et al., 437/169, 192, 195, 200

20. 4,525,383, Jun. 25, 1985, Method for manufacturing multilayer circuit substrate; Tamio Saito, 437/195; 257/750; 427/96, 98; 430/314; 437/192, 228



21. 4,445,267, May 1, 1984, MOSFET Structure and process to form micrometer long source/drain spacing; Francisco H. De La Moneda, et al., 437/41; 257/346, 398; 437/42, 44, 56, 70, 195, 200

22. 4,400,865, Aug. 30, 1983, Self-aligned metal process for integrated circuit metallization; George R. Goth, et al., 437/31; 156/643, 656; 257/517, 587; 437/33, 39, 69, 194, 195, 203, 931

23. 4,398,339, Aug. 16, 1983, Fabrication method for high power MOS device; Richard A. Blanchard, et al., 437/66; 156/648; 257/330; 437/72, 79, 170, 187, 195, 913

24. 4,289,846, Sep. 15, 1981, Process for forming low-reactance interconnections on semiconductors; Earl L. Parks, et al., 430/314; 205/123; 427/96, 560; 430/315, 329; 437/65, 182, 189, 195, 245

25. 4,118,595, Oct. 3, 1978, Crossovers and method of fabrication; Arnold



Pfahnl, et al., 174/256, 261; 257/776; 361/410; 427/96; 430/319; 437/195, 235; 523/443; 524/493 [IMAGE AVAILABLE]

26. 4,113,578, Sep. 12, 1978, Microcircuit device metallization; Louis A. Del Monte, 205/125; 204/192.15, 192.3; 437/183, 194, 195, 230

27. 3,824,678, Jul. 23, 1974, PROCESS FOR LASER SCRIBING BEAM LEAD SEMICONDUCTOR WAFERS; Ronald E. Harris, et al., 437/182; 219/121.73, 121.82; 437/8, 190, 192, 194, 195, 227, 246, 249 [IMAGE AVAILABLE]

28. 3,762,040, Oct. 2, 1973, METHOD OF FORMING CIRCUIT CROSSOVERS; John Andrew Burns, et al., 29/593, 407; 174/261; 228/104, 173.5, 180.2, 212, 243; 257/776; 437/189, 195 [IMAGE AVAILABLE]

29. 3,597,834, Aug. 10, 1971, METHOD IN FORMING ELECTRICALLY CONTINUOUS CIRCUIT THROUGH INSULATING LAYER; Jay W. Lathrop, et al., 437/51; 29/846; 174/257, 260, 261; 257/632, 763, 766, 773; 427/259, 265, 282; 437/189,



195, 230, 246 [IMAGE AVAILABLE]

=> s l1 and 437*192/ccls
667 437*192/CCLS
(437/192/CCLS)
L4 67 L1 AND 437*192/CCLS

=> s l4 and lower conductor